## REMARKS

Claims 1-16 are pending in the application. Claims 1, 8, 12 and 15 have been amended by way of the present amendment. Reconsideration is respectfully requested.

In the outstanding Office Action, claims 1-16 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent No. 6,356,990 (Aoki et al.) and U.S. Patent No. 5,920,888 (Shirotori et al.) and further in view of U.S. Publication No. 2003/0149905 (Santhanam et al) or Huang et al.

### *35 USC Section 103 Rejections*

Claims 1-16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. and Shirotori et al. and further in view of Santhanam et al. Applicant respectfully traverses the rejection.

Independent claims 1, 8, 12 and 15, have been amended to further clarify the invention. In particular, each of the claims have been amended to recite:

> wherein, in a power efficiency access mode, the clock circuit is configured such that the access mode signal enables the HITA signal and the HITB signal to select~~said select signal selects~~ one of said first way and second way to apply clock pulses to at an end of an access cycle, and
>
> wherein, in a high speed access mode, the clock circuit is configured such that the access mode signal disables the HITA signal and the HITB from selecting and both of said first way and second way have clock pulses applied.

Support for the amendment is provided by the original specification and figures. In particular, as shown in **FIG. 4** below, an access mode indication is applied to inverter **33** and when the high speed access mode is selected, AND gates **36** and **37** are enabled in response to each received clock pulse to provide **clock 0** and **clock 1** signals to each of the ways of cache memory **21** (see

**FIG. 1**).[1] Alternatively, as shown in **FIG. 4**, when the high power efficiency mode is selected, comparators **24A** and **24B** enable either AND gate **36** or **37**, through OR gates **34** or **35**, thus providing clocking signals to only one way of the cache memory **21** (see **FIG. 1**).[2]

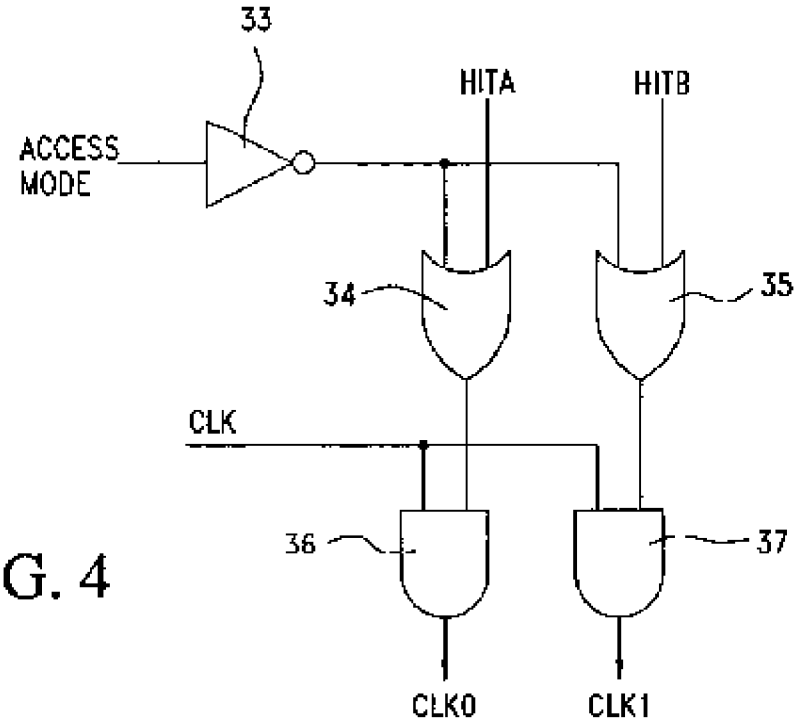


FIG. 4

Therefore, it is respectfully submitted that the amendment raises no question of new matter.

It is respectfully submitted that the applied art of Aoki et al., Shirotori et al. and Santhanam et al., whether taken alone or in combination, do not disclose the claimed invention. The reasoning for this position is presented below.

Aoki et al. discloses a set-associative cache memory having a built-in set prediction array is disclosed.[3] In particular, Aoki et al. discloses the information stored in memory array **21** may

[1] See Specification at **FIG. 4**, paragraph **[0025]**.

[2] *Id.* at **FIG. 4,** and paragraph **[0025]**.

be accessed by an effective address **20**.[4] Further, Aoki et al. discloses the effective address **20** includes a tag field, a line index field, and a byte field.[5] Further, Aoki et al. discloses the tag field of the effective address **20** is utilized to provide cache "hit" information.[6] Furthermore, Aoki et al. discloses the line index field of effective address **20** is utilized to select a specific cache line within memory array **21**, and the byte field of effective address **20** is utilized to index a specific byte within the selected cache line.[7]

Moreover, Aoki et al. discloses a match between a tag from one of two ways in directory **22** and the real page number implies a cache "hit." In addition, Aoki et al. discloses that the cache "hit" signal (i.e., Sel_0 or Sel_1) is also sent to a set-select multiplexor **25** to select an output from one of the two ways of memory array **21**.

However, Aoki et al. is deficient in that it nowhere discloses, as recited in independent claims 1, 8, 12 and 15, the limitation of "applying clock pulses" or "supplying clock signals":

> wherein, in a power efficiency access mode, the clock circuit is configured such that *the access mode signal enables the HITA signal and the HITB signal to select one of said first way and second way to apply clock pulses to at an end of an access cycle*, and
>
> wherein, in a high speed access mode, the clock circuit is configured such that *the access mode signal disables the HITA signal and the HITB from selecting and both of said first way and second way have clock pulses applied* (emphasis added).

In fact, the outstanding Office Action also acknowledges deficiencies in Aoki et al. and attempts to overcome these deficiencies with Shirotori et al.[8] However, Shirotori et al. cannot overcome all of the deficiencies of Aoki et al., as discussed below.

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[3] Aoki et al. at ABSTRACT.
[4] *Id.* at FIG. 2; and column 3, lines 5-6.
[5] *Id.* at FIG. 2; and column 3, lines 6-7.
[6] *Id.* at FIG. 2; and column 3, lines 7-9.
[7] *Id.* at FIG. 2; and column 3, lines 9-14.
[8] Outstanding Office Action at page 3, paragraph 6, lines 14-15.

Shirotori et al. discloses a cache memory that automatically sets a low-, semi-, or high-speed mode of operation according to the result of a comparison between a half-period of a reference clock signal and a pulse width of a reference pulse signal provided by a reference pulse signal generator.[9] However, Shirotori et al. nowhere discloses "applying clock pulses," as explicitly recited in claim 1; or "supplying clock signals," as explicitly recited in claims 8, 12 or 15:

> wherein, in a power efficiency access mode, the clock circuit is configured such that *the access mode signal enables the HITA signal and the HITB signal to select one of said first way and second way to apply clock pulses to at an end of an access cycle*, and
>
> wherein, in a high speed access mode, the clock circuit is configured such that *the access mode signal disables the HITA signal and the HITB from selecting and both of said first way and second way have clock pulses applied* (emphasis added).

[9] Shirotori et al. at ABSTRACT.

In particular, as shown in **FIG. 3** of Shirotori et al. below:

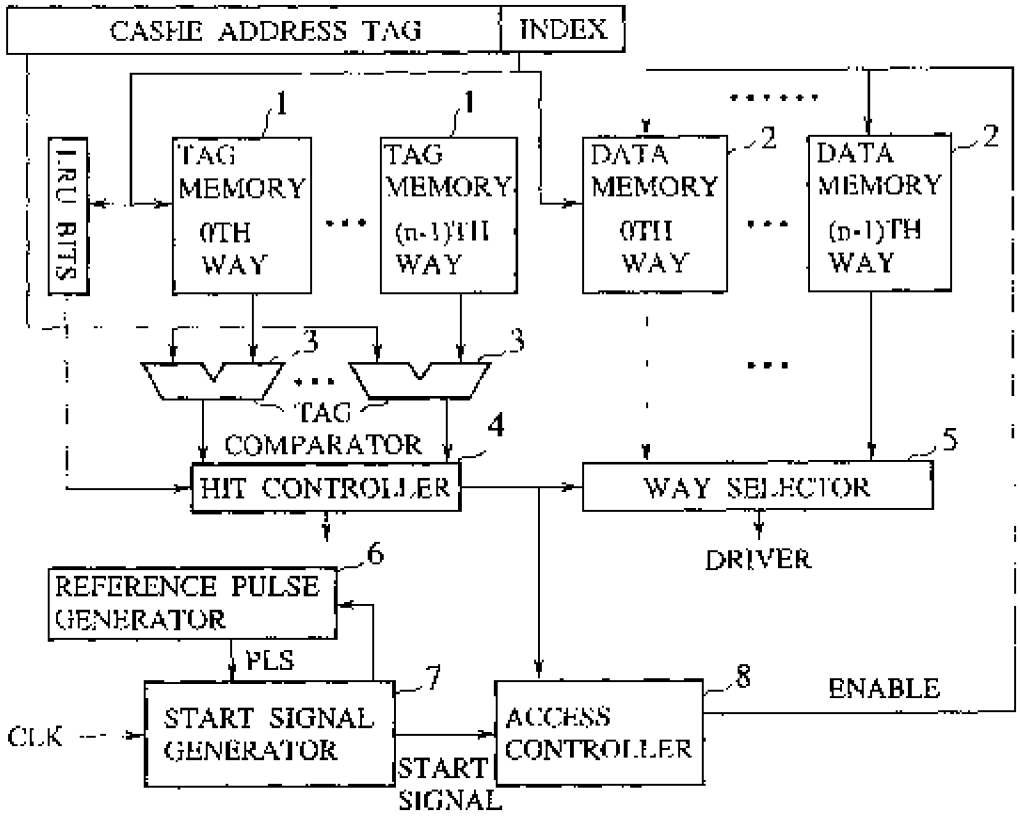


**FIG. 3 of Shirotori et al.**

As shown in **FIG. 3** above, Shirotori et al. discloses: "according to the start signal from the start signal generator **7** and the hit information from the hit controller **4**, the access controller **8** supplies *an enable signal* for allowing the reading of data out of one of the data memories **2** that is associated with the hit tag memory **1**" (emphasis added).[10] More specifically, Shirotori et al. discloses: "upon receiving the hit information, the access controller **8** stops immediately supplying *the enable signal* to the data memories except to the one associated with the hit tag memory **1** so that only the hit data memory **2** is read" (emphasis added).[11]

[10] *Id.* at FIG. 3; and column 4, lines 61-65.
[11] *Id.* at FIG. 3; and column 5, lines 4-7.

However, Shirotori et al. nowhere discloses "applying clock pulses" or "supplying clock signals,":

> wherein, in a power efficiency access mode, the clock circuit is configured such that *the access mode signal enables the HITA signal and the HITB signal to select one of said first way and second way to apply clock pulses to at an end of an access cycle*, and
>
> wherein, in a high speed access mode, the clock circuit is configured such that *the access mode signal disables the HITA signal and the HITB from selecting and both of said first way and second way have clock pulses* (emphasis added).

That is, Shirotori et al. nowhere discloses: (1) "applying clock pulses" or "supplying clock signals"; (2) nor that the recited "clock pulses" or "clock signals" are: in accordance with the clock circuit being in the "high speed" or "high efficiency," access mode, as recited in amended claim 1 or claims 8, 12 and 15.

With regards to element (1) above, Shirotori et al., as explicitly recited above and as can be clearly seen in **FIG. 3** above, *only* discloses supplying a single "enable signal" to the ways **2**. Shirotori et al. nowhere discloses applying "clock pulses" or supplying "clock signals" as does the claimed invention. In fact, it is respectfully submitted that the "enable signal" of Shirotori et al. is non-periodically alternated between an "on" or "off" signal level. In contrast, the "clock pulses" or "clock signals" of the claimed invention with are periodic and have defined cycle, as is consistent with a pulse or clock signal.

With regards to element (2) above, Shirotori et al., as can be clearly seen in **FIG. 3** above, *nowhere* discloses all three signals (i.e., "access mode signal," "HITA signal" and "HITB signal," as recited in claims 1, 8, 12 and 15) for "applying" or "supplying" to a clock circuit (e.g., the "START SIGNAL GENERATOR" **7** of **FIG. 3** of Shirotori et al).

Moreover, as shown **FIG. 1** of the specification below, both of the above patentably distinguishable differences between Shirotori et al. and the claimed invention are illustrated. In particular, as discussed above, as recited in the claims and as shown in **FIG. 1**, the claimed

invention includes: a clock circuit **20** that receives three signal inputs: (1) "ACCESS MODE"; (2) "HITA"; and "HITB." Moreover, as recited in the claims: in response to an "access mode signal," a "HITA signal" and a "HITB signal" where these three signals determine whether "applying clock pulses" or "supplying clock signals" from the clock circuit **20** of "one or both ways" (i.e.,. "WAY0" or "WAY1" **21**) occurs in accordance with a "high frequency" or "high efficiency," access mode. Thus, in consideration of the above discussion, it is respectfully submitted that Shirotori et al. cannot overcome all of the deficiencies of Aoki et al.

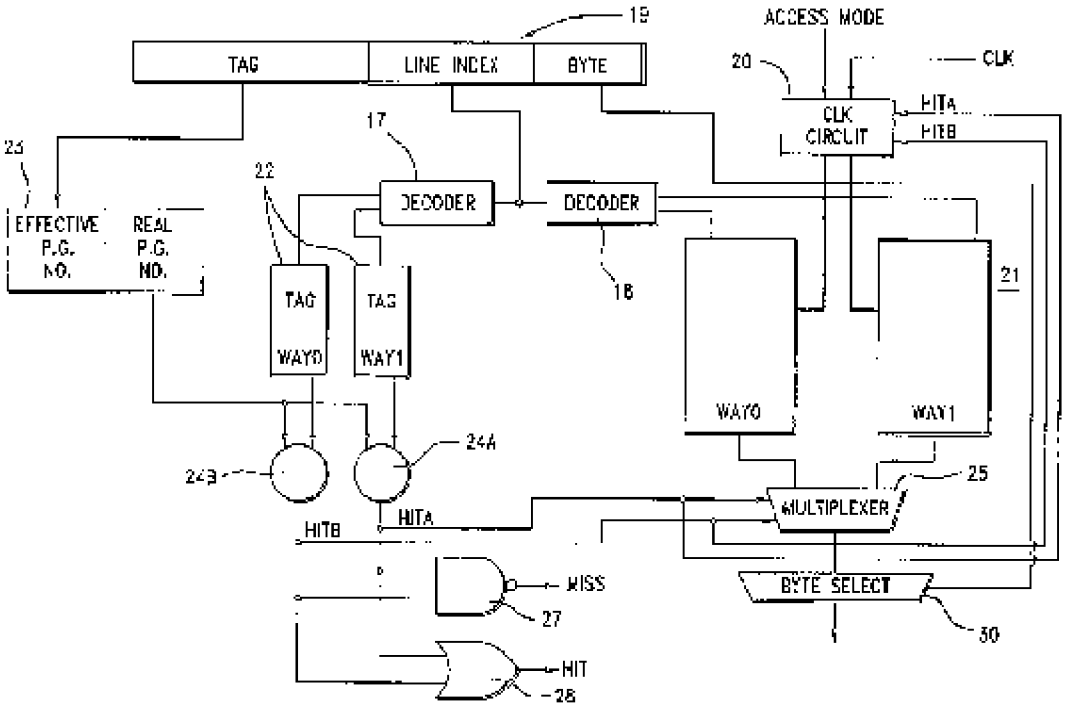


**FIG. 1 of US Application No. 10/714,105**

In addition, the outstanding Office Action acknowledges the combination of Aoki et al. and Shirotori et al. is deficient and attempts to overcome these deficiencies with Santhanam et al. or Huang et al.[12] However, neither Santhanam et al. nor Huang et al. can overcome all of the deficiencies of Aoki et al. and Shirotori et al., as discussed below.

[12] Outstanding Office Action at page 5, paragraph 6, lines 37-38.

Santhanam et al. discloses a processor may include an execution circuit, an issue circuit coupled to the execution circuit, and a clock tree for clocking circuitry in the processor.[13] In particular, Santhanam et al. discloses a data cache **30** may be a circuit with multiple subcircuits (e.g. cache banks) that may be conditionally clocked individually dependent on which bank is accessed by a given load/store instruction.[14] Further, Santhanam et al. discloses the cache banks may be collectively clocked dependent on whether or not a load/store instruction has been issued and has not reached the cache access stage.[15]

However, Santhanam et al. nowhere discloses: "applying clock pulses" or "supplying clock signals", as recited in independent claims 1, 8, 12 and 15:

> wherein, in a power efficiency access mode, the clock circuit is configured such that *the access mode signal enables the HITA signal and the HITB signal to select one of said first way and second way to apply clock pulses to at an end of an access cycle*, and
>
> wherein, in a high speed access mode, the clock circuit is configured such that *the access mode signal disables the HITA signal and the HITB from selecting and both of said first way and second way have clock pulses* (emphasis added).

That is, in the same manner as discussed previously, Santhanam et al. nowhere discloses "applying clock pulses" or "supplying clock signals"; to one or both of said ways as recited in claims 1, 8, 12 and 15, in accordance with whether the clock circuit is in a "high efficiency" or "high speed" access mode as recited in the claimed invention. Thus, Santhanam et al. cannot be used to overcome all of the deficiencies of Aoki et al. and Shirotori et al. Moreover, for similar reasoning, the disclosure of Huang et al. also cannot overcome all of the deficiencies of Aoki et al. and Shirotori et al.

Therefore, it is respectfully submitted that none of Aoki et al., Shirotori et al., Santhanam et al. nor Huang et al., whether taken alone or in combination, disclose, suggest or make obvious

[13] Santhanam et al. at ABSTRACT.
[14] *Id.* at FIG. 1; paragraph **[0058]**; lines 4-7.
[15] *Id.* at FIG. 1; paragraph **[0058]**; lines 7-10.

the claimed invention and that claims 1, 8, 12 and 15, and claims dependent thereon, patentably distinguish thereover.

***Conclusion***

Applicant believes no fee is due with this response. However, if a fee is due, please charge Deposit Account No. 50-0563, under Order No. 20421-00071-US from which the undersigned is authorized to draw.

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Respectfully submitted,

Electronic signature: /Myron Keith Wyche/
Myron Keith Wyche
Registration No.: 47,341
CONNOLLY BOVE LODGE & HUTZ LLP
1875 EYE Street, N.W., Suite 1100
Washington, DC 20006
(202) 331-7111 (Tel)
(202) 293-6229 (Fax)
Agent for Applicant